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# DESIGN OF FULL ADDER USING DOUBLE GATE MOSFET

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**Abstract:** With the continuous scaling of CMOS technology, short-channel effects, leakage currents, and power dissipation have become significant challenges in VLSI circuit design. To overcome these limitations, this work presents the design of a full adder using Double Gate MOSFET (DG-MOSFET) technology. DG-MOSFETs offer superior electrostatic control over the channel by utilizing two gates, which effectively suppress short-channel effects and improve device performance. The proposed full adder circuit is designed to achieve low power consumption, reduced propagation delay, and improved switching characteristics compared to conventional CMOS-based designs. By leveraging the advantages of double gate structure, the circuit exhibits better current drive capability and reduced leakage currents. Simulation results demonstrate that the DG-MOSFET-based full adder provides enhanced performance in terms of speed, power efficiency, and reliability, making it suitable for next-generation nano-scale integrated circuits and high-performance computing applications.

**Keywords:** Double Gate MOSFET (DG-MOSFET), Full Adder, VLSI Design, Low Power Design, Nanoelectronics, Multi-Gate Transistors, CMOS Scaling, Short Channel Effects, Leakage Power Reduction, High-Speed Arithmetic Circuits, Digital Logic Design, Propagation Delay, Energy Efficient Circuits, Integrated Circuits (ICs), Advanced Semiconductor Devices.

**INTRODUCTION:** VLSI systems are having many operations like fundamental arithmetic operation in addition is one of the common and widely used operations. Such as arithmetic operations are subtraction, multiplication, division, address calculation etc. Utilizing binary adders the full adder is structured and enhancing 1-bit full adders execution assumes a vital job in VLSI. Distinctive assortments of full adders abuse totally unique rationale structures and advances. The battery which is having demand of current history the devices are driven and portable, low power and area efficient devices they must need an implementation. As indicated the multiplying module focus upon silicon wafer in every 3 years by Moore's law. In this system of interconnection limited circuit are having thickness on a chip, therefore transistor door length is decreased to huge dimension. The structured applications of today are in the range 2nm. Chip is essential and basic piece of numerous items are required for ordinary. For example, home apparatuses, radio and PCs frameworks. Span of transistor was confined in wonders short channel impacts are incorporate of bearer impact of hot, gate prompted hindrance bringing down, impact and burrowing of oxide thickness. In corruption of gadget execution and gadget lifetime at littler door length is because of expanded electric field. The central piece of chip of a transistor. Chief test was minuscule issues at nanometer go is ultra rapid; control dissemination and supply voltage. Lower control prompts lesser power supplies, less exceptional batteries [2]. Low power and High speed are the plan exchange offs in VLSI industry. As far back as its beginning, the plan of full adders which shapes the essential building squares of all computerized VLSI circuits has been experiencing a significant enhancement, being roused by three fundamental structure objectives, viz. limiting the transistor tally, limiting the power utilization and expanding the speed. Most of the VLSI applications, for example, advanced flag preparing and microchips, utilize number-crunching activity. Expansion, subtraction, augmentation, and increase and collect (MAC), are instances of the most normally utilized activities. The development of compact gadgets like PDAs, PDAs, and so on, request fast handling capacities that additionally expend less power. The1-bit full adder is the building square of these activity modules. In this way, improving its execution is basic for upgrading the general module execution. In this paper, we present a novel 1-bit full-adder cell utilizing XOR- XNOR circuit, which offers quicker activity, and devours less power than the other proposed full-viper cell dependent on XOR- XNOR gate [1]. The structure paradigm in a full adder cell was normally different overlap. The transistor tally was, obviously, an essential concern which to a great extent influences the plan intricacy of many capacity units, for example, Algorithmic rationale unit (ALU) and multiplier. The restricted power supply capacity of present battery innovation has made power utilization a vital figure in convenient gadgets. The restricted by the size of the transistors, parasitic capacitance and postponement the speed of the plan in the basic way [3]. Capacity of driving was a full adder is imperative, since, full adders are generally utilized in course setup, where the yield of one gives the contribution to other. On the off chance that the full adders need driving ability, at that point it requires extra support, which therefore builds the power scattering significant enhancement in power utilization, speed and size, however at the expense of feeble driving capacity and decreased voltage swing. In any case, decreased voltage swing has the benefit of lower control utilization. At first the hardware began their advancement with the innovation of vacuum tubes. Be that as it may, with the assistance of Vacuum tubes just the development of electrons was contemplated. After vacuum tubes transistors and diodes were presented. Be that as it may, for bigger circuits it was hard to manufacture them in a board as they involved bigger space and devoured more power. The full adder circuit execution is subject to the methodology for structuring the circuit. The speed of activity of a circuit is in a roundabout way found with the assistance of defer time figuring which specifically relies upon the transistor check, the rationale profundity and

other criteria. The power utilization relies upon the exchanging movement and the number and the transistor estimate. The transistor measure and steering multifaceted nature knows the territory of a kick the bucket. Circuit acknowledgment for low zone has turned into a vital issue with the development of incorporated circuit towards high combination thickness and high working frequencies. Because of the critical pretended by XOR-XNOR gate in different circuits particularly in number-crunching circuits, streamlined structure XOR-XNOR circuit to accomplish little size and deferral is required. The essential worry to structure XOR-XNOR door is to get low power utilization and postponement in the basic way and full yield voltage swing with low number of transistors to execute it. An overview of writing uncovers a wide range of various sorts of XOR-XNOR doors that have been acknowledged throughout the years. The early structures of XOR-XNOR gates depended on either 4 transistors or 3 transistors that are expectedly utilized in many plans [4]. Full viper goes about as the essential square of all adders which are utilized to perform multi bit increases. There are additionally different approaches to plan the Full Adder circuit as far as CMOS rationale [5]. With expanding request in speed and power, our principle point is to configuration Full adder circuit so it devours less power and quicker. The vast majority of the power in any circuit is being devoured by the power given to the information way of the circuit which comprises of the transistors. Subsequently by lessening the quantity of transistors we can decrease the power utilization additionally by diminishing the information way, the circuit can be made quicker.

**RELATED WORK** The testing criteria of the rising low power and fast correspondence computerized flag preparing chips can be tended to by investigating the very much designed profound submicron transistor advancements. The execution of the fundamental number circuits to actualize complex calculations, for example, convolution, relationship and advanced sifting, characterizes the execution of numerous greater modules of Digital Signal Processors (DSPs). The semiconductor business has seen a touchy development of mix of modern interactive media based applications into portable hardware gadgetry since the most recent decade. Be that as it may, control utilization is the basic region of worry in this field and must be diminished for a specific working recurrence. Also, there is a drive by creators to take a stab at littler silicon territory, higher speed, longer battery life, and upgraded dependability in light of dangerous development of interest and prominence of convenient electronic items. The motivation behind coordinated hardware is to pack complex electronic circuits in least territory with decrease in power dispersal and postponement. With the period of innovative progression, diminishing the quantity of transistors and ultra-low power configuration has turned into the main thrust for mix of an ever increasing number of uses without acquiring any overhead as far as silicon region. The execution of configuration is significantly represented by three essential variables viz. zone multifaceted nature, postpone execution and consistency of interconnection. The consistency of interconnection implies the manner in which transistors are set down, directing of interconnects in the most ideal way and conforming to the tenets of format. Territory of the circuit likewise relies upon the interconnection of wires which exhaust the greater part of the region of a VLSI circuit. Diverse rationale styles have been proposed throughout the years with an exchange off of one execution angle to the detriment of other. The circuit delay is influenced by the quantity of transistors in arrangement, wiring interconnections identified with wiring capacitances, transistor sizes and number of reversal levels. Full adder usage can be accomplished by utilizing it is possible that one rationale style or more than one rationale style. The XOR-XNOR circuits are fundamental building hinders in different circuits' particularly number juggling circuits (adders and multipliers), blowers, comparators, equality checkers, code converters, mistake recognizing or blunder remedying codes and stage identifier. The adders and multipliers being the quick number continuously calculation cells and generally utilized for some circuits of VLSI configuration are the regular research zones. A further expansion to unwavering quality and bundling issue issues have been brought with the ascent up in chip thickness and increment in power utilization of VLSI frameworks. Bundling and cooling cost of VLSI frameworks likewise runs up with high power dispersal. These days, low power utilization alongside least postponement and zone necessities is one of vital plan thought for IC originators.

Circuit acknowledgment for low power and low territory has turned into a vital issue for the development of incorporated circuit towards exceptionally high joining thickness and high working frequencies. Because of the imperative pretended by XOR and XNOR doors in different circuits particularly in number continously circuits, improved plan of XOR and XNOR circuit to accomplish low power, little size and low deferral is required. The essential worry to plan XOR-XNOR gate is to get low power utilization and postponement in the basic way and right yield having the least number of transistors to execute the voltage swing. XOR gate is a basic building square of advanced circuits and there is constant research proceeding to upgrade its execution. Along these lines, as far back as its origin, the structure of XOR gates frames the fundamental building square of all advanced VLSI circuits which has been experiencing a significant enhancement, being spurred by three essential plan objectives, viz. limiting the transistor tally, diminishing the power utilization and expanding the speed. Hosseinzadeh underscored that the circuit execution can be enhanced through transistor tally minimization. XOR gates assume an imperative job in advanced frameworks including math circuits, encryption circuits, comparator, equality checker, etc. Upgrading the execution of the XOR gates can altogether enhance the execution of these circuits. Many plan structures and procedures have been created to plan XOR doors with decrease in power utilization. The writing study uncovers a wide range of XOR gates that have been acknowledged throughout the years. The predominant worry to structure XOR door is to procure right yield voltage swing with least number of transistors and furthermore, execution with low power utilization and postponement in the basic way

EXISTED SYSTEM : The below figure (1) demonstrates the engineering of existed framework. The non full-swing XOR/XNOR circuit which is appeared in fig (1) has the power and delay as far as productive. This structure has a yield voltage drop issue for just a single information legitimate esteem of its besides. To tackle this issue and give an ideal structure to the entry way of the XOR/XNOR, in the circuit appeared in Fig.

1 was proposed. In the full swing the structure of the yield of this, the all conceivable info mixes. The basic way of the circuit on NOT gates does not have of the existed system of XNOR/XOR.

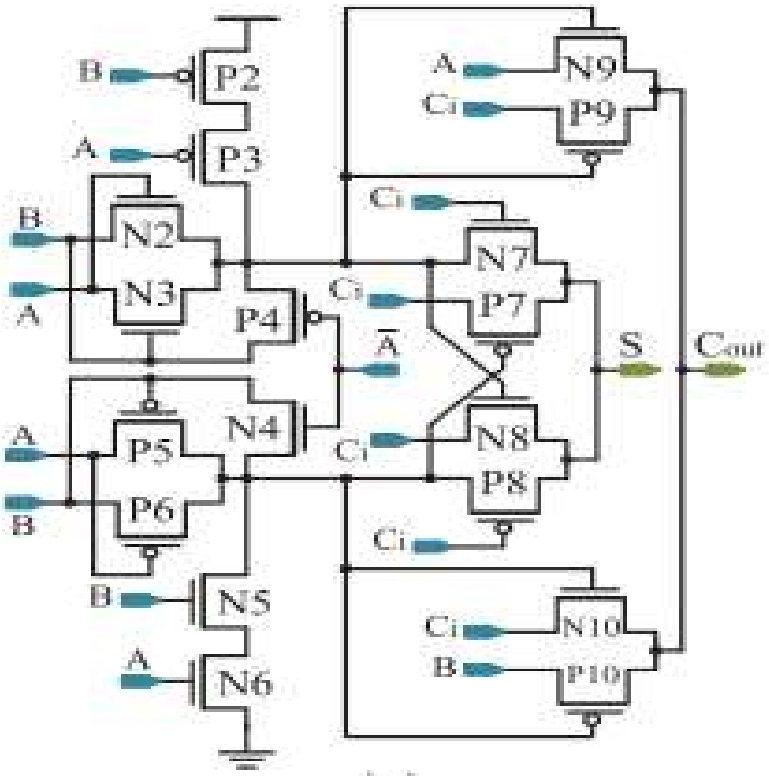


**Fig. 1: EXISTED SYSTEM**

The data sources are as per the following An and B which are denoted as the capacitances of the XOR circuit. These are not symmetric on the grounds side and one of these two should be related with the commitment of NOT gate. In the same way another should be related with the scattering of nMOS transistor. In addition, the data capacitances of transistors N2 and N3 are not equal in the perfect situation (least PDP). Generally, the information relationship with transistors N2 and N3 won't impact the limit of the circuit. Hence, it is more brilliant to relate the data A, which is moreover connected with the NOT passages and to the transistor with smaller information capacitance. By doing this, the information capacitances are progressively symmetrical, and thusly, the delay and power usage of the circuit will be lessened. To light up which transistor (N2 or N3) has greater data capacitance, let us consider the condition that the wellsprings of information change from AB = 00 to AB = 10.

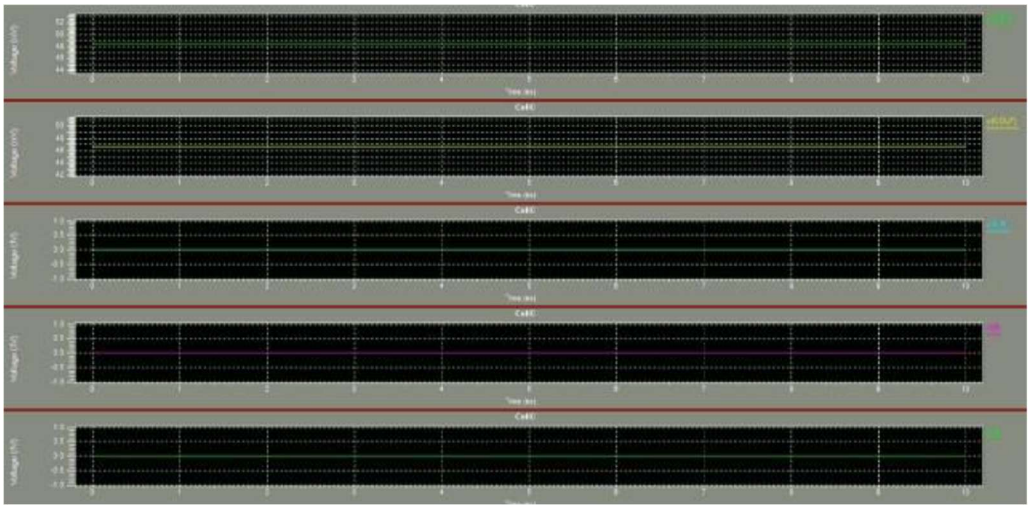

Fig. 2: EXISTED OUTPUT WAVEFORM

PROPOSED SYSTEM:

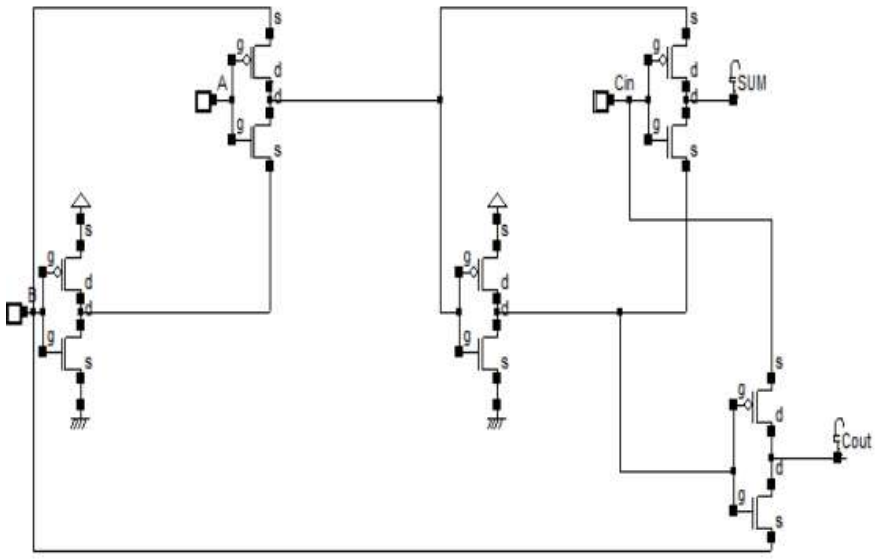


Fig. 3: PROPOSED DESIGN

The above figure (3) shows the design of proposed system. The full adder comprises of two modules, including one XOR-XNOR door, and two multiplexers. The creators give XOR-XNOR gates to enhance the execution of full adders. , these XOR and XNOR doors give awful yield rationale levels for certain information blends. This issue can be tackled by controlling the (W/L) proportions of PMOS and NMOS transistors, which reestablishes the rationale levels to a worthy dimension. Basically, the XOR/XNOR gate produces the intensity in the full adder cell. Hence the power utilization is decreed by the full adder cell with the planning. The XOR/XNOR gates will be used in different computerized applications. In this system we use eight transistors for better purpose. Here NOT gate is used in the circuit of grounds of NOT cells. These cells should drive the delay in basic formation level. Depend on the logic style of transistor the circuits operate its function. In this circuit the power utilization is superior. The XOR-XNOR signals are mainly associated with the full adder circuits. The XOR-XNOR contributes its signals by using multiplexers. Consequently, two concurrent signs with a similar postponement are important to keep away from glitches in the yield hubs of the FA. In this structure, the yields have been driven just by nMOS transistor, and along these lines, two pMOS transistors are associated with yields (XOR and XNOR) as cross coupled to recoup the yield level voltages. The main issue in the XOR-XNOR circuits is having cross coupled structure. This structure will expand the intensity of the system. Not only intensity, the measure of transistor is also expanded to a level. By using two NOT gates in the system is a big issues in the system. Hence the outputs of XOR and XNOR gates will practically diminish the output stage. But the proposed system gives effective results compared to existed system.

RESULTS

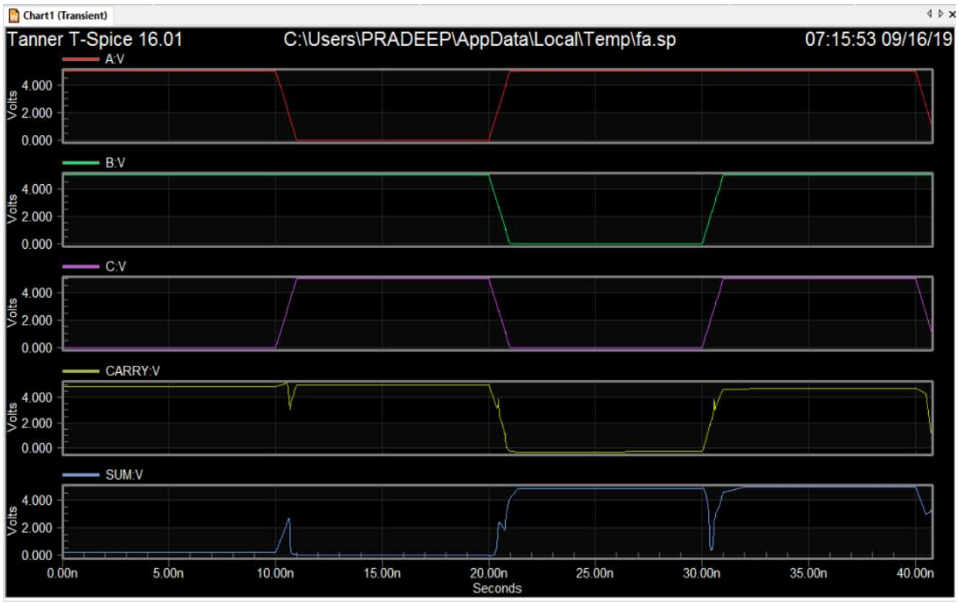


Fig. 4: OUTPUT WAVEFORM

In the proposed system, the number of transistors used is 20 and in existed system, the number of transistors used is 10.

Advantages

- Reduced Short-Channel Effects:
  Better control over the channel minimizes threshold voltage variation and leakage.
- Low Power Consumption:
  Reduced leakage currents lead to improved energy efficiency.
- High Speed Operation:
  Faster switching due to improved gate control and carrier transport.
- Improved Scalability:
  Suitable for nano-scale technologies beyond conventional CMOS limits.
- Better Electrostatic Control:
  Dual gates enhance control over channel potential.
- Higher Drive Current:
  Increased current capability improves overall performance.
- Reduced Propagation Delay:
  Faster carry and sum generation in arithmetic operations.

Applications

- Arithmetic Logic Units (ALU)
- Digital Signal Processing (DSP) Systems
- Microprocessors and Microcontrollers
- Low Power VLSI Circuits
- Portable and Battery-Operated Devices
- High-Speed Computing Systems
- Nanoelectronics and Advanced IC Design

Conclusion

The design of a full adder using Double Gate MOSFET technology demonstrates significant improvements over conventional CMOS-based designs. The dual-gate structure effectively reduces short-channel effects and leakage currents, resulting in lower power consumption and enhanced performance. The proposed design achieves reduced propagation delay and improved switching behavior, making it highly suitable for modern VLSI applications. Overall, DG-MOSFET-based full adders provide a promising solution for future integrated circuit design, particularly in nano-scale technologies where power efficiency and performance are critical. The results validate that adopting advanced device structures can significantly enhance digital circuit efficiency.

Future Scope

- Integration with FinFET and Multi-Gate Devices:
  Extend the design to FinFET or Gate-All-Around (GAA) technologies.
- Implementation in Lower Technology Nodes:
  Explore performance in 7nm, 5nm, and beyond.
- Optimization Using Advanced Logic Styles:
  Combine DG-MOSFET with GDI or pass transistor logic for further improvements.
- Low-Power Design Techniques:
  Incorporate power gating and clock gating methods.
- Design of Complex Arithmetic Circuits:
  Extend the approach to multipliers, adders (CLA, CSA), and ALUs.

**References:**

[1] J. P. Colinge, *FinFETs and Other Multi-Gate Transistors*, New York, NY, USA: Springer, 2008.
[2] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, 2nd ed., Cambridge, U.K.: Cambridge Univ. Press, 2009.
[3] B. Razavi, *Design of Analog CMOS Integrated Circuits*, New York, NY, USA: McGraw-Hill, 2001.
[4] N. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed., Boston, MA, USA: Addison-Wesley, 2011.
[5] A. Mukherjee, S. Mukhopadhyay, and K. Roy, "Modeling and analysis of double-gate MOSFET for low power applications," *IEEE Trans. Electron Devices*, vol. 52, no. 6, pp. 1234–1242, Jun. 2005.
[6] S. Bobba et al., "Design of double-gate MOSFET-based logic circuits," *IEEE Trans. Nanotechnology*, vol. 6, no. 2, pp. 234–240, Mar. 2007.
[7] R. H. Dennard et al., "Design of ion-implanted MOSFETs with very small physical dimensions," *IEEE J. Solid-State Circuits*, vol. 9, no. 5, pp. 256–268, Oct. 1974.
[8] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proc. IEEE*, vol. 91, no. 2, pp. 305–327, Feb. 2003.
[9] V. Zhirnov and R. Cavin, "Nanoelectronics: Negative capacitance and beyond CMOS devices," *IEEE Computer*, vol. 41, no. 1, pp. 37–43, Jan. 2008.
[10] A. Chandrakasan, N. Verma, and D. Daly, "Ultralow-power electronics for biomedical applications," *Annu. Rev. Biomed. Eng.*, vol. 10, pp. 247–274, 2008.
[11] S. Narendra and A. Chandrakasan, *Leakage in Nanometer CMOS Technologies*, New York, NY, USA: Springer, 2006.
[12] H. Iwai, "Roadmap for 22 nm and beyond (invited paper)," *Microelectronic Engineering*, vol. 86, no. 7–9, pp. 1520–1528, 2009.
[13] C. H. Diaz et al., "Double-gate MOSFET technology: Device design and scalability," *IEEE Electron Device Lett.*, vol. 24, no. 6, pp. 345–347, Jun. 2003.
[14] S. Borkar, "Design challenges of technology scaling," *IEEE Micro*, vol. 19, no. 4, pp. 23–29, Jul. 1999.
[15] M. Alioto, "Energy-quality scalable adders," *IEEE Trans. Circuits Syst. I*, vol. 64, no. 1, pp. 87–100, Jan. 2017.